# 40Gb/s QSFP+
# Active Breakout Copper Cable

APCA04-QSCXXX-yy

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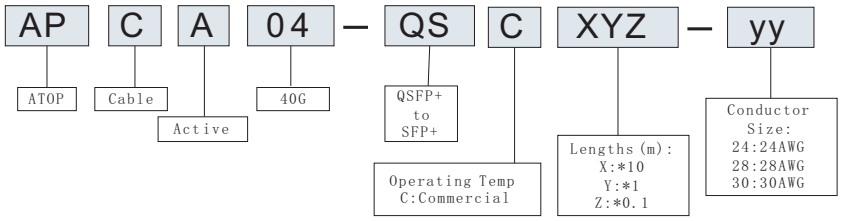
## Product Features

- ✓ Available in lengths of 1 to 10m
- ✓ Four-channel full-duplex active copper
- ✓ cable with breakout from QSFP+ to four SFP+
- ✓ Hot-pluggable footprint
- ✓ RoHS compliant and Lead Free
- ✓ Single power supply 3.3V, low power consumption
- ✓ Commercial operating temperature optional
- ✓ Compliant with QSFP + and SFP+ MSA
- ✓ Fully comply with IEEE802.3ba and QDR specifications

## Applications

- ✓ 10/40G Ethernet
- ✓ Data storage
- ✓ Fibre channel
- ✓ Switch, router
- ✓ Serial data transmission

## Product Selection



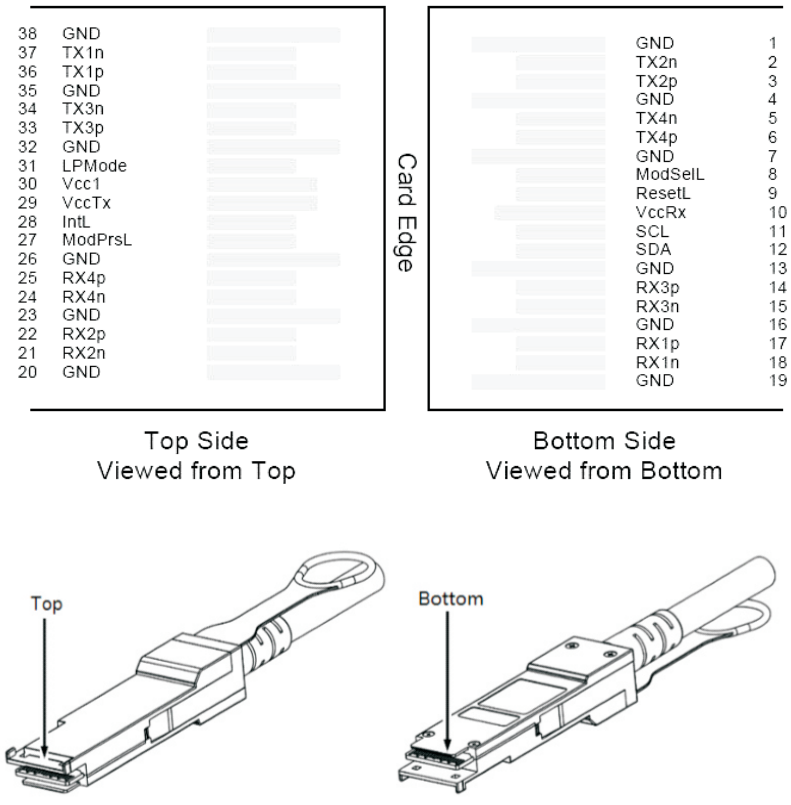

| Part Number | Lengths | Wire Size |
|---|---|---|
| APCA04-QSC010-30 | 1m | AWG30 |
| APCA04-QSC020-30 | 2m | AWG30 |
| APCA04-QSC030-30 | 3m | AWG30 |
| APCA04-QSC050-30 | 5m | AWG30 |
| APCA04-QSC070-30 | 7m | AWG30 |
| APCA04-QSC080-28 | 8m | AWG28 |
| APCA04-QSC100-28 | 10m | AWG28 |

*For availability of additional cable lengths, please contact ATOP.

## Pin Descriptions

| Pin | Symbol | Name | Ref. |
|---|---|---|---|
| 1 | GND | Ground | |
| 2 | Tx2n | Transmitter Inverted Data Input, CML-I | |
| 3 | Tx2p | Transmitter Non-Inverted Data output, CML-I | |
| 4 | GND | Ground | |
| 5 | Tx4n | Transmitter Inverted Data Input, CML-I | |
| 6 | Tx4p | Transmitter Non-Inverted Data output, CML-I | |
| 7 | GND | GND | |
| 8 | ModSelL | The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on asingle 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the "High" state in the module | |
| 9 | ResetL | The ResetL pin must be pulled to Vcc in the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. | |
| 10 | VccRx | + 3.3V Power Supply Receiver | |
| 11 | SCL | 2-Wire Serial Interface Clock | |
| 12 | SDA | 2-Wire Serial Interface Data | |
| 13 | GND | GND | |
| 14 | Rx3p | Receiver Non-Inverted Data Output, CML-O | |
| 15 | Rx3n | Receiver Inverted Data Output, CML-O | |
| 16 | GND | GND | |
| 17 | Rx1p | Receiver Non-Inverted Data Output, CML-O | |
| 18 | Rx1n | Receiver Inverted Data Output, CML-O | |
| 19 | GND | Ground | |
| 20 | GND | Ground | |
| 21 | Rx2n | Receiver Inverted Data Output, CML-O | |
| 22 | Rx2p | Receiver Non-Inverted Data Output, CML-O | |
| 23 | GND | Ground | |
| 24 | Rx4n | Receiver Inverted Data Output, CML-O | |
| 25 | Rx4p | Receiver Non-Inverted Data Output, CML-O | |

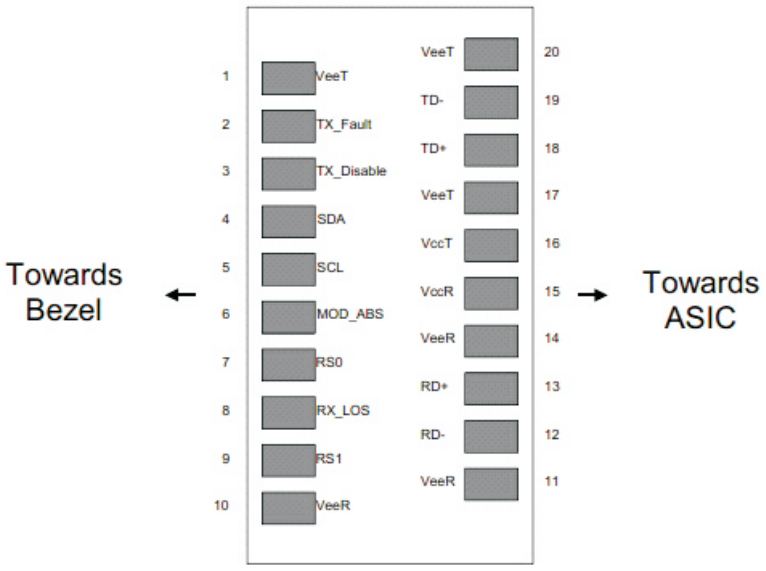
| | | |
|---|---|---|
| 26 | GND | Ground |
| 27 | ModPrsL | Module Present, connect to GND |
| 28 | IntL | The IntL pin is an open collector output and must be pulled to host supply voltage on the host board. The INTL pin is de-asserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read. |
| 29 | VccTx | +3.3 V Power Supply transmitter |
| 30 | Vcc1 | +3.3 V Power Supply |
| 31 | LPMode | The LPMode pin shall be pulled up to Vcc in the QSFP+ module. This function is affected by the LPMode pin and the combination of the Power_over-ride and Power_set softwarecontrol bits (Address A0h, byte 93 bits 0,1). |
| 32 | GND | Ground |
| 33 | Tx3p | Transmitter Non-Inverted Data Input, CML-I |
| 34 | Tx3n | Transmitter Inverted Data Output, CML-I |
| 35 | GND | Ground |
| 36 | Tx1p | Transmitter Non-Inverted Data Input, CML-I |
| 37 | Tx1n | Transmitter Inverted Data Output, CML-I |
| 38 | GND | Ground |

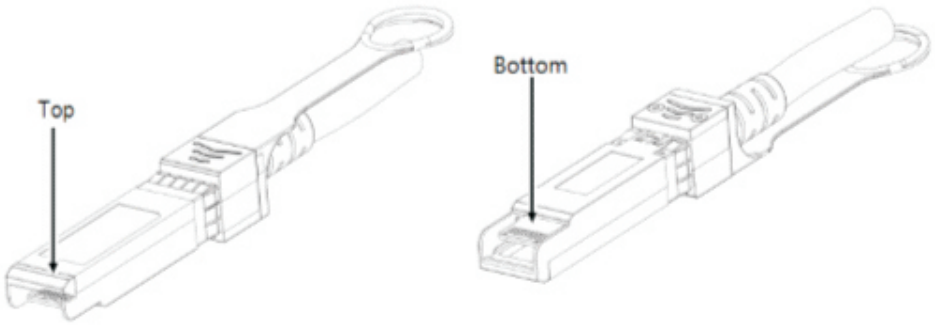



Pin-out of Connector Block on Host Board

## SFP+ end

| Pin | Symbol | Name/Description | Ref. |
|---|---|---|---|
| 1 | VeeT | Transmitter Ground (Common with Receiver Ground) | |
| 2 | TX Fault | Transmitter Fault. LVTTL-O | |
| 3 | TX Disable | Transmitter Disable. Laser output disabled on high or open. LVTTL-I | |
| 4 | SDA | 2-Wire Serial Interface Data Line (Same as MOD-DEF2 in INF-8074i). LVTTL-I/O | |
| 5 | SCL | 2-Wire Serial Interface Data Line (Same as MOD-DEF2 in INF-8074i). LVTTL-I | |
| 6 | Mod_ABS | Module Absent, Connect to VeeT or VeeR in Module. | |
| 7 | RS0 | Rate Select 0, optionally controls SFP+ module receiver LVTTL-I | |
| 8 | LOS | Loss of Signal indication. Logic 0 indicates normal operation. LVTTL-O | |
| 9 | RS1 | Rate Select 1, optionally controls SFP+ module transmitter. LVTTL-I | |
| 10 | VeeR | Receiver Ground (Common with Transmitter Ground) | |
| 11 | VeeR | Receiver Ground (Common with Transmitter Ground) | |
| 12 | RD- | Receiver Inverted DATA out. AC Coupled. CML-O | |
| 13 | RD+ | Receiver Non-inverted DATA out. AC Coupled. CML-O | |
| 14 | VeeR | Receiver Ground (Common with Transmitter Ground) | |
| 15 | VccR | Receiver Power Supply | |
| 16 | VccT | Transmitter Power Supply | |
| 17 | VeeT | Transmitter Ground (Common with Receiver Ground) | |
| 18 | TD+ | Transmitter Non-Inverted DATA in. AC Coupled. CML- I | |
| 19 | TD- | Transmitter Inverted DATA in. AC Coupled. CML- I | |
| 20 | VeeT | Transmitter Ground (Common with Receiver Ground) | |






Pin-out of Connector Block on Host Board

## Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ | Max | Unit | Ref. |
|---|---|---|---|---|---|---|
| Maximum Supply Voltage | Vcc | -0.5 | | +4.0 | V | |
| Storage Temperature | TS | -4.0 | | +85 | °C | |
| Operating Humidity | RH | 0 | | 85 | % | |

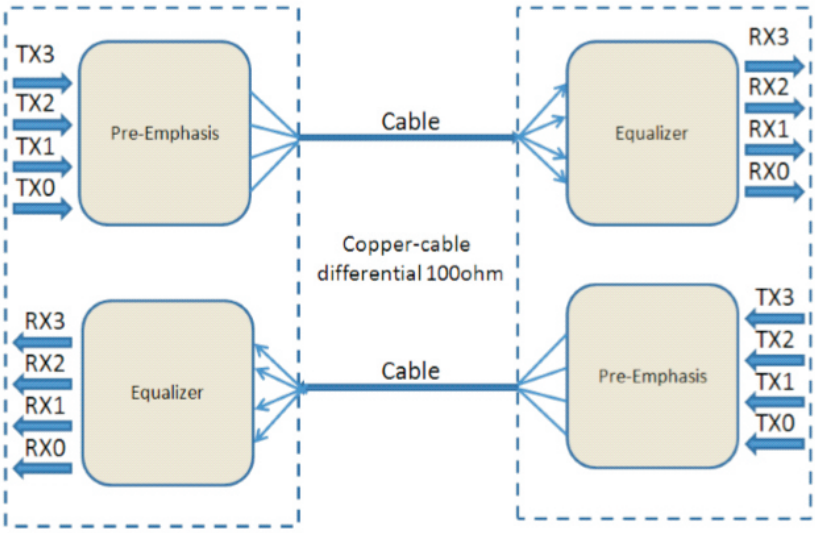
## Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Ref. |
|---|---|---|---|---|---|---|
| Power Supply Voltage | Vcc | 3.13 | 3.30 | 3.47 | V | |
| Case Operating Temperature | Tc | 0 | - | +70 | °C | Commercial |
| Bit Rate Each Lane | Br | 1 | - | 11.3 | Gbps | |
| Length | Lmax | 1 | - | 10 | m | |

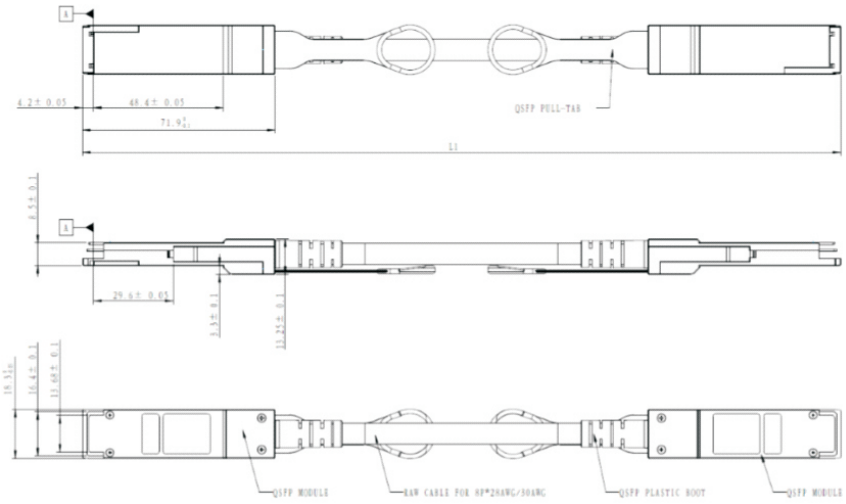
## Cable specifications

| Parameter | Symbol | Min | Typ | Max | Unit | Ref. |
|---|---|---|---|---|---|---|
| Sizes | Rin | 30 | | 28 | AWG | |
| impedance | Z | 90 | 100 | 110 | Ohm | |

## Product block diagram




## Mechanical Specifications



Unit: mm
Tolerance: ± 0.2mm

## Revision History

| Revision | Initiated | Reviewed | Approved | DCN | Release Date |
|---|---|---|---|---|---|
| Version1.0 | Tang zhiqiang | Li Tao | Ding zheng | New Released. | Nov 22, 2019 |

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